

Notice of Allowability	Application No.	Applicant(s)
	10/618,650	KONDOH, HIROSHI
	Examiner Long K. Tran	Art Unit 2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. This communication is responsive to 04/03/2006.
2. The allowed claim(s) is/are 1, 2, 3, 5 – 7, 18, 21 – 26 and 29 – 45.
3. Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some* c) None of the:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
5. CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) hereto or 2) to Paper No./Mail Date _____.
 - (b) including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. Notice of References Cited (PTO-892)
2. Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date 2/27/06, 3/28/06
4. Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. Notice of Informal Patent Application (PTO-152)
6. Interview Summary (PTO-413),
Paper No./Mail Date _____.
7. Examiner's Amendment/Comment
8. Examiner's Statement of Reasons for Allowance
9. Other _____.

Response to Amendment

1. This office action is in response to Amendment filed on 04/03/2006.
2. Claims **4, 8 – 17, 19 – 20, 27, 28** and **46** have been cancelled.
3. Claims **1, 24** and **25** have been amended.
4. Claims **1, 2, 5 – 7, 18, 21 – 26** and **29 – 45** are presented for examination.

Information Disclosure Statement

5. This office acknowledges of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on 02/27/2006 and 03/28/2006.

The references cited on the PTO -1449 form have been considered.

EXAMINER'S AMENDMENT

6. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mr. Nikolaus P. Schibli on June 12, 2006.

The application has been amended as follows:

Claims:

Claim 1 (Currently Amended): A semiconductor device, comprising'.
a gate electrode;
an insulating layer on the gate electrode;
a first electrode on the insulating layer;

a second electrode on the insulating layer at an interval with the first electrode;
an organic semiconductor layer disposed in the interval between the first
electrode and the second electrode, [and] covering and contacting at least part of the
first electrode and the second electrode; end

a first resistance layer formed on the organic semiconductor layer and having an
electrical resistance lower than an electrical resistance of the organic semiconductor
layer; and

a second resistance layer formed at least at one of the position between the first
resistance layer and the organic semiconductor layers the position between the first
electrode and the organic semiconductor layer, and the position between the second
electrode and the organic semiconductor layer,

wherein the first resistance layer is formed from a metal selected from the group
consisting of chromium (Cr), tantalum (Ta), titanium (Ti), copper (Cu), aluminum (Al),
molybdenum (Mo), tungsten (W), nickel (Ni), gold (Au), palladium (Pd), platinum (Pt),
silver (Ag), or tin (Sn), and

wherein the second resistance layer has an electrical resistance so that carriers
in the organic semiconductor layer are allowed to tunnel through the second resistance
layer when a voltage of a predetermined value or more than the predetermined value is
applied across the second resistance layer.

Claim 3 (Amended): A semiconductor device, comprising:

a gate electrode;
an insulating layer on the gate electrode;

a first electrode on the insulating layer;
a second electrode on the insulating layer at an interval with the first electrode;
an organic semiconductor layer disposed in the interval between the first electrode and the second electrode,[and] covering and contacting at least part of the first electrode and the second electrode; and
a first resistance layer formed on the organic semiconductor layer and having an electrical resistance lower than an electrical resistance of the organic semiconductor layer,
wherein one of the first electrode and the second electrode is in contact with the first resistance layer.

Claim 29 (Amended): A liquid crystal display device, comprising a semiconductor device including:
a gate electrode;
an insulating layer on the gate electrode;
a first electrode on the insulating layer;
a second electrode on the insulating layer at an interval with the first electrode;
an organic semiconductor layer disposed in the interval between the first electrode and the second electrode,[and] covering and contacting at least part of the first electrode and the second electrode; and
a first resistance layer formed on the organic semiconductor layer and having an electrical resistance lower than an electrical resistance of the organic semiconductor layer,

wherein one of the first electrode and the second electrode is in contact with the first resistance layer.

Claim 30 (Amended): A calculating device, comprising at least one of a NOT circuit, a NAND circuit, and a NOR circuit each including a plurality of semiconductor devices,

each of the semiconductor devices including:

a gate electrode;

an insulating layer on the gate electrode;

a first electrode on the insulating layer;

a second electrode on the insulating layer at an interval with the first electrode;

an organic semiconductor layer disposed in the interval between the first electrode and the second electrode, [and] covering and contacting at least part of the first electrode and the second electrode; and

a first resistance layer formed on the organic semiconductor layer and having an electrical resistance lower than an electrical resistance of the organic semiconductor layer,

wherein one of the first electrode and the second electrode is in contact with the first resistance layer

Allowable Subject Matter

7. Claims 1, 2, 5 – 7, 18, 21 – 26 and 29 – 45 are allowed.
8. The following is an examiner's statement of reasons for allowance: Claims 1, 2, 5 – 7, 18, 21 – 26 and 29 – 45 are allowable over the prior art of record because none of

the prior art whether taken singularly or in combination, especially when these limitations are considered within the specific combination claimed, to teach:

An organic semiconductor layer disposed in the interval between a first electrode and a second electrode and covering at least part of the first electrode and the second electrode, and a first resistance layer being contacted with one of the first electrode and the second electrode as cited in the independent claims 1, 3, 29 and 30; a second resistance layer being formed at least one of the position between the first resistance layer and the organic semiconductor layer, the position between the first electrode and the organic semiconductor layer, and position between second electrode and the organic semiconductor layer and carriers in the organic semiconductor layer allowed to tunnel through the second resistance layer when a voltage equal or more than a voltage of predetermined value being applied across the second resistance layer as cited in the independent claim 1; and among other limitations as cited in the independent claims 1, 3, 29 and 30.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long K. Tran whose telephone number is 571-272-1797. The examiner can normally be reached on Mon-Thu.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MinSun Harvey or Matthew Smith can be reached on 571-272-1835 or 571-272-1907 (Smith). The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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June 12, 2006